IN THE CLAIMS

Cancel claims 1-11 without prejudice or disclaimer, and add new claims 12-19 as follows:

1-11. (Canceled).

12. (New) A semiconductor device formed on a semiconductor chip comprising:

a first circuit block supplied with a first operating voltage;

a second circuit block supplied with a second operating voltage;

a voltage generating circuit generating a third operating voltage in response to said first operating voltage; and

a third circuit block supplied with said third operating voltage;

wherein said voltage generating circuit includes a fourth circuit that changes the characteristics of the third operating voltage against said first operating voltage when said first operating voltage is higher than a first voltage.

13. (New) The semiconductor device according to claim 12, wherein said first operating voltage is higher than said second operating voltage.

14. (New) The semiconductor device according to claim 13, wherein said third operating voltage is lower than said first operating voltage.

15. (New) The semiconductor device according to claim 14, wherein said first voltage is a voltage higher than a voltage used for normal operation and wherein said fourth circuit controls the third operating voltage when aging test is operated.

16. (New) The semiconductor device according to claim 14, wherein said third circuit block further includes a charge pump circuit and a regulator circuit;

wherein said charge pump circuit receives said first operating voltage and outputs a voltage inputted to said regulator circuit,

wherein said regulator circuit includes a plurality of diodes and a first transistor;

wherein said plurality of diodes are which is coupled in series between an output of said charge pump circuit and said source/drain path of said first transistor;

wherein said third operating voltage is outputted from an output of said first transistor.

17. (New) The semiconductor device according to claim 16,

wherein said plurality of diodes comprise a plurality of second transistors which have the same thickness of gate insulators of third transistors used in input and output circuits.

18. (New) The semiconductor device according to claim 17,

wherein said second transistors are N type MOS transistors.

19. (New) The semiconductor device according to claim 16,

wherein said third circuit block comprises a memory array having a plurality of DRAM memory cells.